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TI 78/90
Time Code Generator Chip STUDER TCGA

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Technical Information

APPLICATION NOTES

1. General

The STUDER TCGA (Time code generator adapter) is a SMPTE/EBU standard LTC generator in a VLSI 44 pin package. The chip is build in CMOS technology and features TTL compatible in/outputs.

The Time Code Generator Adapter TCGA is a peripheral device which can be directly connected to the 6800/6803 MPU bus without any additional circuitry.

The device can be software-programmed by the MPU to satisfy a wide variety of time code based applications.

The TCGA generates different time code formats such as 24, 25, and 30 frames plus drop frame and has facilities to accept control commands for the time code rate and direction control (reverse TC generation). This control is effected by the MPU program. Additionaly , the MPU can start and stop the time code generation or "freeze" the time code (in this case the generator will continuously send a constant time code data pattern).

TC -data, user bits, the TC-frame bit position as well as the unused bits in the TC block can be preset.

The device has 4 software selectable time code clock reference inputs. Depending on application, the signal frequency at these inputs can be controlled using 16-bit dividers (divide by M+1, N+1, and K+1 counters) or a "multiply by 2" circuits, see Block diagram. The internal TCGA select logic allows for the selection of frequency dividers or multiplier. Thus the Tc rate can be programmed; the maximum is 100 x times playspeed (E clock frequency 1 MHz).

The synchronization of the TCGA to the reference signals of the different video, digital audio or film standards requires only one external PLL circuit (see Fig. 2). Fig. 2 shows the two different PLL configurations which are supported using the internal select logic and the programmable dividers of the TCGA. The device has an external control input which - if enabled by the MPU - may be used to synchronize the beginning of the time code generation to an external event.

The TCGA allows the time code data, user bits data, the bit position or the unused bits of the time code frame to be preset during the stop or running state of the TCGA, by writing into the appropriate data buffers/registers. Constant time code data streams may be generated by writing the data to the Time Code Data Buffer and using the command "freeze time code ".

The chip contains also a 16-bit up/down tape (move pulse) counter.

2. TCGA OPERATION

(see BLOCK DIAGRAM, Fig. 7)

PLL Count Modifier Registers

The PLL Count Modifier Registers (K, N - Register) are 16-bit write - only registers (see Table 1). The MPU can preset the 16-bit K and N -values by writing the LSB and MSB data into the corresponding 8 - bit registers. The write operation to the MSB register will cause the 16 bit value to be transferred into the 16 bit counter/divider.

TABLE 1

REGISTER	DATA	ADDRESS
K	LSB MSB	00 [hex] 01 [hex]
N	LSB MSB	02 [hex] 03 [hex]

These registers may be used to program the external PLL to function as a frequency multiplier or divider (see Fig. 2).

The frequency of the TCGA clock signal F_G is calculated using the following formula:

$$F_G = \frac{(N+1)}{(K+1)} \times F_R \qquad (N, K: 0..65535)$$

N and K are the 16 bit values loaded into the registers N respectively K. F_R is the frequency of the external reference signal. The circuit shown in Fig. 2 covers a range of the input reference signal frequences which can be applied to the PLL to generate the corresponding synchronous time code signal at the TCGA time code output TC. Table 2 shows some typical values.

TABLE 2

Typical frequencies F_R which are used to synchronize a time code generator. The nominal TC - rates F_{TC} are: 1920 Hz (24 Frames), 2000 Hz (25 Frames), 2400 Hz (30 Frames), 2397,6 Hz (Drop frame). The values N+1 and K+1 in the table must be calculated for $F_G=2F_{TC}$

F_R:		(N+1)/(K+1) 24 Frames	25 Fr.	30 Fr.	Drop Fr.
Video: (PAL)	15,625	68/3125	32/125	960/3125	3966/13021*
[kHz] (NTSC)	15,73425	5120/20979	16000/62937	6400/20979	32/105
(30Fr)	15,750	128/525	16/63	32/105	1332/4375
Dig. Audio:	32,0	3/25	2/16	3/20	2997/20000
[kHz]	37,8	32/315	20/189	8/63	999/7875
	44,0559	3200/36713*	500/5507*	4000/36713*	16/147
	44,1	64/735	40/441	16/147	1998/18375
	48,0	4/50	2/48	2/20	999/10000
Line:	50	384/5	160/2	192/2	11998/125
[Hz]	60	128/2	200/3	160/2	999/25

Note *): TC-clock frequency errors 1.38, 0.59, 0.2, 0.74 Fr/hour respectively

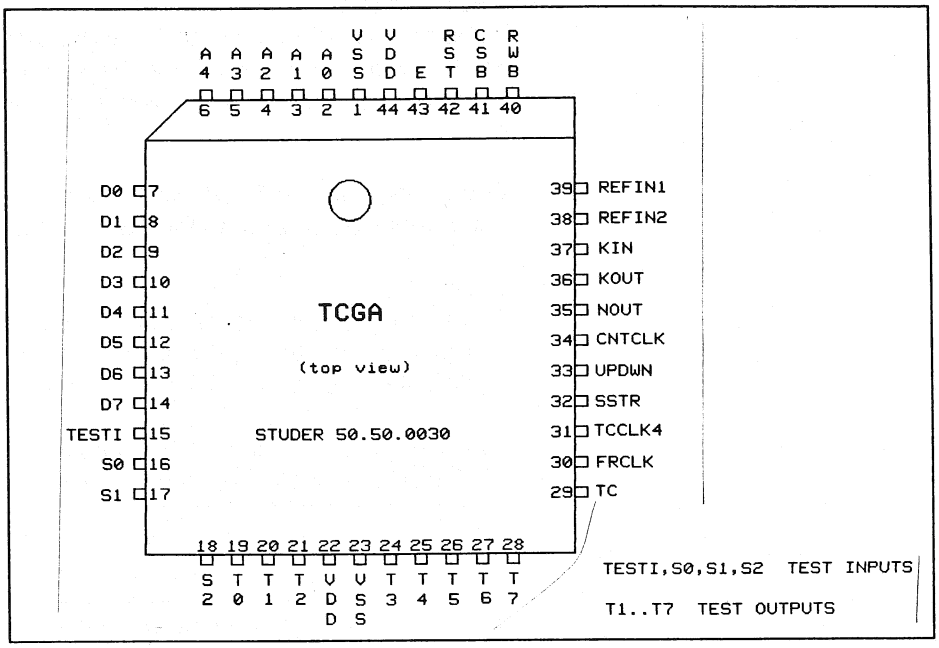


Fig. 1.: TCGA pin layout

Time Code Rate Register

(M-Register), Addr. 04[hex], 05[hex].

The M-Register can be used for Time Code rate (vary-speed) control of the TCGA. The local reference signal frequency, applied to the REFIN1 pin, will be divided by the 16-bit value M+1. The MPU can preset the value M by writting into the address locations 04H (LSB) and 05H (MSB). The write operation to the MSB register will cause the 16-bit value to be transferred into the 16-bit counter.

16-BIT UP/DWN COUNTER

Addr. 11[hex], 12[hex]

The UP/DWN Counter counts the positive transitions on its input CNTCLK. The 16-bit counter value will be incremented or decremented depending on the state of the UPDWN input. The counter will count up if UPDWN input is "high". The 16-bit counter value can be read or written by the MPU. Both address locations (11[hex] for LSB and 12[hex] for MSB) must be accessed by the MPU during the write or read operation. The address location 11[hex] (LSB) must be accessed first.

Generator Command Register

Addr. 07[hex]

The Generator Command Register is a write-only register which is used by the MPU to start or stop the Time Code generation, define the Time Code direction (up/down), enable Start Strobe Input SSTR and freeze the Time Code Data.

bit0: start/stop
If this bit is set to "1", the TCGA will start to generate the Time Code Signal at the TC - output. To stop the generator, this bit must be cleared.

bit1: direction
This bit is used to provide the direction select for the generated Time Code ("0" forward, "1" reverse).

bit2: SSTR enable

If this bit and bit 0 are set to "1" at the same time, the positive transition at the SSTR input will initialize the beginning the Time Code generation. The generator will stay in the running state until the bit 0 has been cleared by the MPU.

Please note that the TCGA will accept the SSTR signal only if the start/stop bit (bit 0) was cleared prior to the SSTR enable command.

bit3: freeze

This bit may be used to freeze the Time Code Data at the TC output. If this bit and bit 0 are set to "1", the TCGA will continuosly transmit the constant Time Code Data which can be initialized by writing to the Time Code Data Buffer.

Additionally, bit 6 and bit 7 of the Command Register can be used to select the TCGA Time Code clock reference (see Table 3).

TABLE 3

bit 7	bit 6	TC-Clock Reference (see Blockdiagram)
0	0	REFIN1 (divide by M+1)
0	1	REFIN1 (multiply by 2)
1	0	REFIN2
1	1	KIN (divide by K+1)

The Generator Command Register will be cleared by a hardware reset (RST-Input).

TC - Bit Position Register

Addr. 06[hex]

The TC - Bit Position Register is a 7-bit register, used as a pointer to one of the 80 Time Code Data Bits of the Time Code Frame. During the Time Code generation, this register is automatically incremented or decremented to point to the next TC data bit. By writing to this register, the MPU may change the pointer value allowing the TCGA to be synchronized with the accuracy of the one Time Code bit period .

TC - Data Preset Buffer

The TC - Data Preset Buffer consists of 4 write-only registers (see Table 4).

TABLE 4

Register	Address
FRAMES	08[hex]
SECONDS	09[hex]
MINUTES	0A[hex]
HOURS	0B[hex]

The contents of the registers must be binary coded data.

Example:

Time: 10 hrs, 12 min, 18 sec, 24 frs
Register contents: 18[hex] (fr), 12[hex] (sec), 0C[hex] (min), 0A[hex] (hr)

To transfer the Time Code Data from the TC-Preset Buffer into the corresponding Time Code counters, the register 0B[hex] (hours) must be accessed at the end of the MPU write sequency.

UB - Data Buffer

Like the TC - Data Preset Buffer, the UB (user bits) - Data Buffer consists of 4 write only registers (see Table 5).

TABLE 5

Register	Address
UB - GROUPS 1,2	0C[hex]
3,4	0D[hex]
5,6	0E[hex]
7,8	0F[hex]

TC - Format Register

Addr. 10[hex]

The TC - Format Register is a write-only register which defines the TCGA Time Code format:

TABLE 6

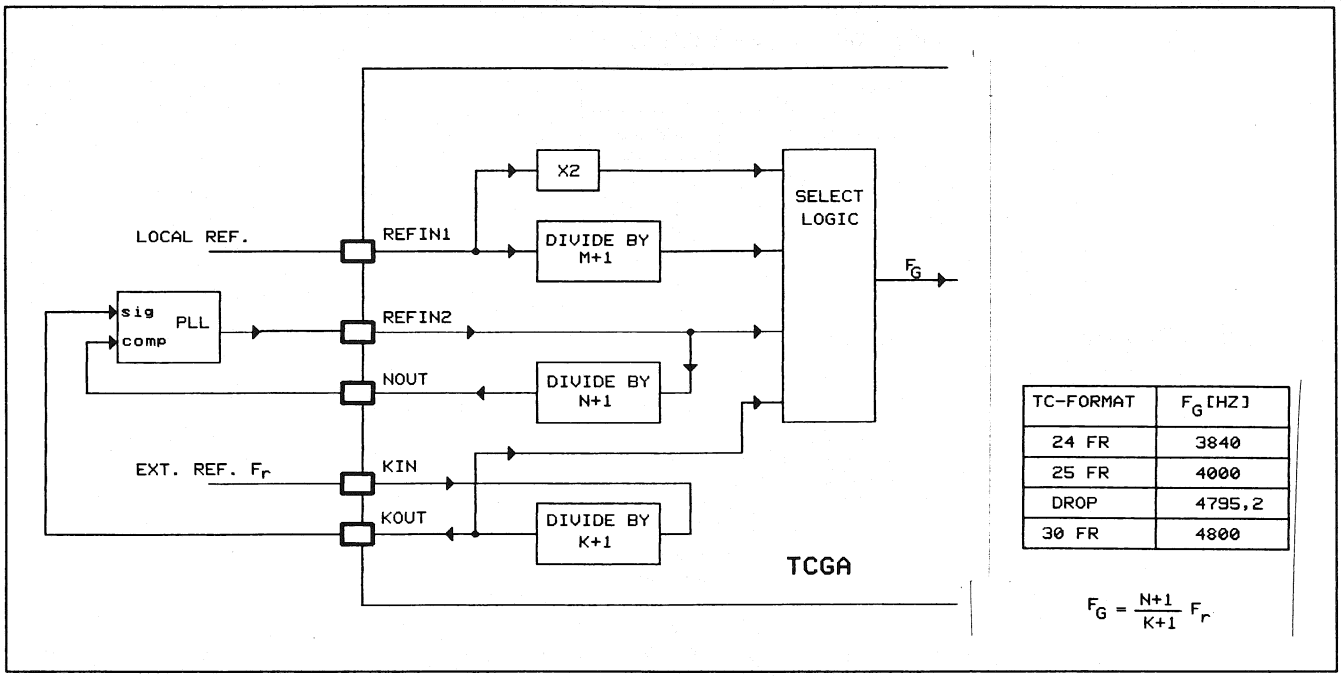
bit 1	bit 0	TC - FORMAT
0	0	24 Fr/sec
0	1	25 Fr/sec
1	0	30 Fr/sec
1	1	Drop-Frame

Additionaly, bit2 - bit6 may be used by the MPU to write the data into the Time Code bits which are not defined by the SMPTE standard.

TABLE 7

Register bit:	TC bit:
2	11
3	27
4	43
5	58
6	59

This register will be cleared by a hardware reset.



TC-FORMAT	F_G [HZ]
24 FR	3840
25 FR	4000
DROP	4795,2
30 FR	4800

$$F_G = \frac{N+1}{K+1} F_r$$

Fig. 2a: Typical TCGA application using external PPL, config. 1

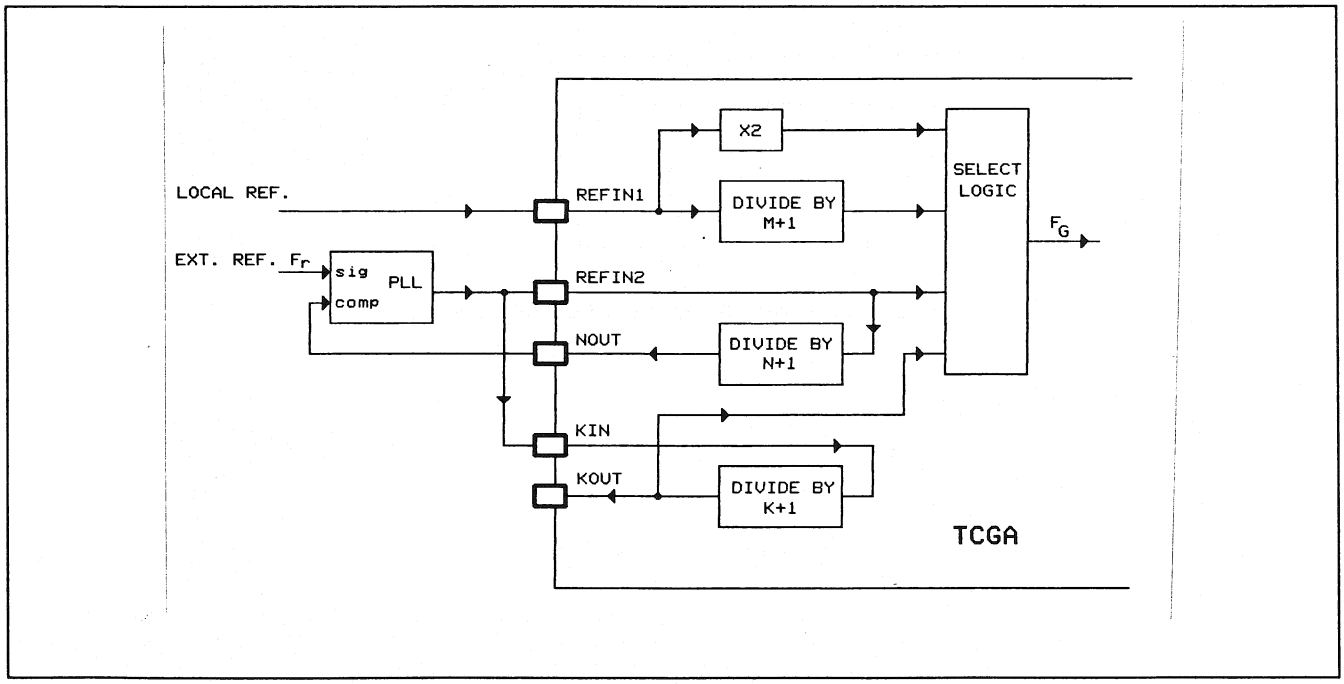


Fig. 2b: Typical TCGA application using external PPL, config. 2

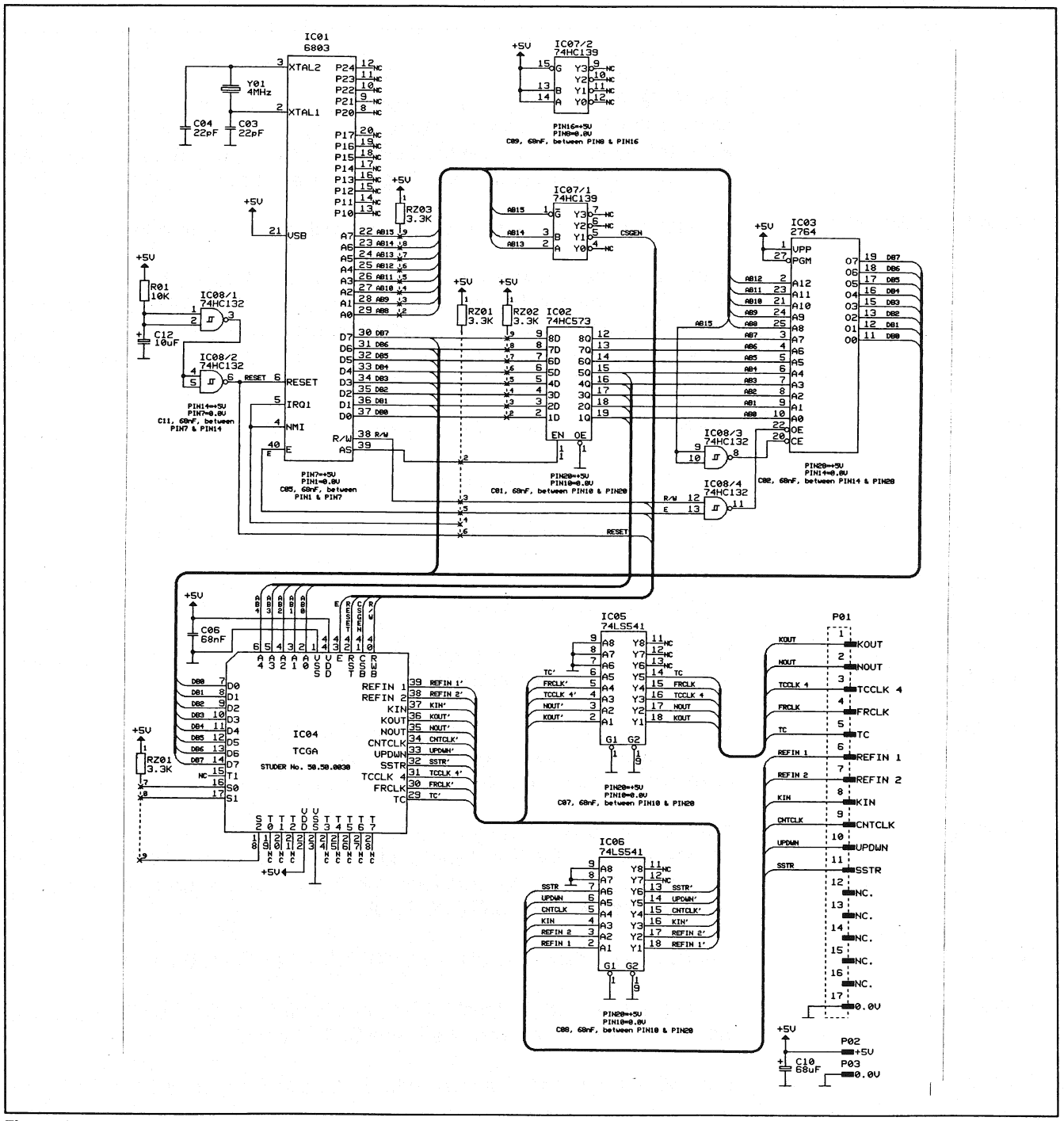


Fig. 3.: Application Example

3. Signal functions

SSTR

The SSTR (Start Strobe) is a positive edge sensitive input used to initialize the start of the Time Code generation. In order for Start Strobe transition to be accepted by the TCGA, both the Start/Stop bit (bit0) and Start Strobe Enable bit (bit2) of the Generator Command Register have to be set.

REFIN1, REFIN2, KIN

The REFIN1, REFIN2 and KIN are the external time code clock inputs.

Because of the synchronous design of the TCGA logic, the maximum signal frequency which may be applied at the inputs REFIN1, REFIN2 and KIN depends on the frequency of the E clock. The frequency of any of the reference signals must not exceed 50% of the E clock frequency value (25% if "multiply by two" circuit is selected as a reference input).

NOUT

The NOUT is the output of the programmable divide by N+1 16-bit counter.

KIN

The KIN is the input of the programmable divide by K+1 16-bit counter.

KOUT

The KOUT is the corresponding output of the K divider/counter.

RST

Reset input, active "low". If activated, it will cause the Command Register and Format Register to be cleared.

E, RWB, CSB, A0...A4, D0...D7

The specification of these inputs/outputs will meet the timing requirements of the Motorola 6801/03 microprocessor.

CNTCLK

The CNTCLK is the clock input for the 16-bit UP/DWN counter, internally synchronized by the negative edge of the E signal. The counter will be incremented or decremented by the positive transition of the CNTCLK.

UPDWN

It is the input used to control the 16-bit UP/DWN Counter. The counter will be incremented if UPDWN is "high" and and decremented if UPDWN is "low". To avoid any counter timing violations, this input must not be changed during the positive transition of the CNTCLK signal.

TC

The TC is the serial output of the SMPTE/EBU Time Code Data.

FRCLK

The active "low" output signal FRCLK, one Time Code Bit Period long, is used to indicate the end of the transmitted Time Code Frame.

TCCLK4

The TCCLK4 is the the Time Code Generator clock output signal.

4. DC-ELECTRICAL CHARACTERISTIC

The TCGA is a custom CMOS IC (gate array) with full input/output TTL compatibility.

All input buffers have pull-up resistors. The drive capability of the output buffers is 4mA. The 3-state I/O buffers (4mA drive capability) are used to drive the bidirectional Data Bus D0..D7.

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

V_{DD}	DC Supply Voltage	-0,3V to +7V
V_{IN}	DC Input Voltage	-0,3V to V_{DD} + 0,3V
I_{IN}	DC Input Current	± 10mA
T_{stg}	Storage Temperature	- 40 °C to + 125 °C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

V_{DD}	DC Supply Voltage	4,75V to 5,25V
T_A	Ambient Temperature	0 °C to 70 °C

DC ELECTRICAL CHARACTERISTICS (specified at V_{DD} = +5V ±5%)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High Level Input Voltage		2,0		V
V_{IL}	Low Level Input Voltage			0,8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD}$	-10	10	uA
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$	- 200	- 10	uA
V_{OH}	High Level Output Voltage	I_{OH} = -4mA	2,4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 4mA		0,4	V
I_{OZ}	High Impedance Leakage Current	$V_{OUT} = V_{DD}$ or V_{SS}	- 200	- 10	uA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}		100	uA

5. POWER DISSIPATION

There are three main sources for the power dissipation of the TCGA:

- the AC power dissipated by the output load (application dependent)
- the DC power dissipated by the TTL compatible input buffer
- the AC power dissipated by the internal gates

The AC power dissipated by the internal gates may be calculated using the following equation:

$$P_{int} = PG \times N \times F \times A$$

where:

PG = power per gate [10µW ··(1/gate) · (1/MHz)]
N = the total number of gates [5500]
F = the operating frequency [in MHz] (the frequency of the E clock signal, 1 .. 5MHz)
A = the activity of the circuit, typically 0,2 (equivalent to 20 %). Factor A depends completetly on the mode of application, as not all nodes of the circuit are changing in every cycle.

6. TEST LOGIC

Although the inputs S0..S2 and outputs T0..T7 are used for testing the TCGA - ASIC, they may be also used in applications. Any byte of the actually generated Time Code Data can be selected by the select inputs S0..S2 and continuously read at the data outputs T0..T7 (see Table 8).

TABLE 8

Select Code S2	S1	S0	SMPTE/EBU - LTC Data Bits T7	...	T0
0	0	0	b7	...	b0
0	0	1	b15	...	b8
0	1	0	b23	...	b16
0	1	1	b31	...	b24
1	0	0	b39	...	b32
1	0	1	b47	...	b40
1	1	0	b55	...	b48
1	1	1	b63	...	b56

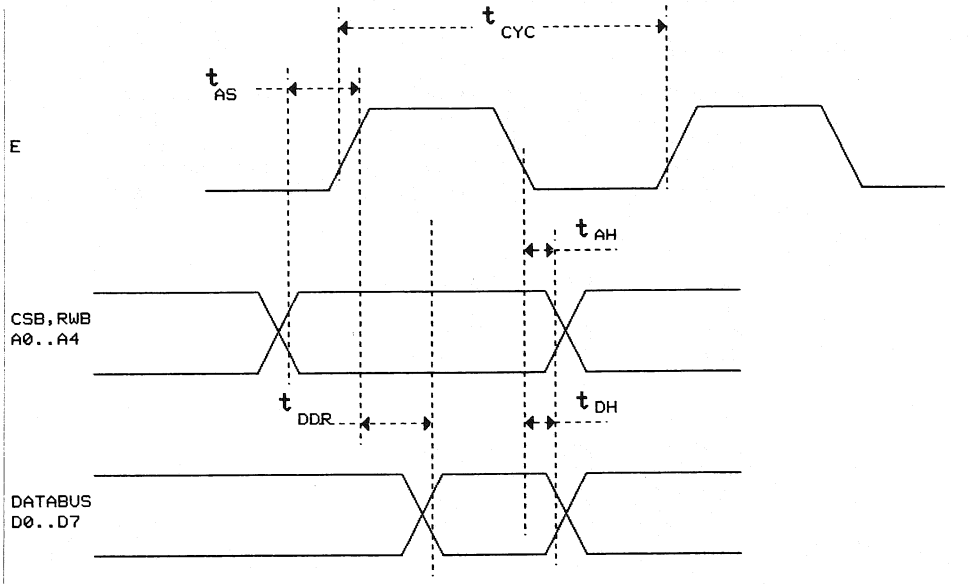
7. SOFTWARE EXAMPLE. INITIALIZATION OF THE TCGA

The following code sample shows the initialization of the TCGA for a typical applicaton (see Fig. 3). The reference signal (200 kHz) will be applied to the input pin REFIN1.

(6803 Assembler)

```
* Define the TCGA Registers (see Fig. 3)
*
                          M_REG_LSB     EQU   02004[hex]      M-Register (LSB)
                          M_REG_MSB     EQU   02005[hex]                 (MSB)
                          CMD_REG       EQU   02007[hex]      Command Register
                          BIT_CNT       EQU   02006[hex]      TC-Bit Counter
                          TC_FORM_REG   EQU   02010[hex]      TC-Format Register
*
* Define Time Code Data Buffer
*
                          FRAME         EQU   02008[hex]
                          SEC           EQU   02009[hex]
                          MIN           EQU   0200A[hex]
                          HOUR          EQU   0200B[hex]
*
* Define UB Data Buffer
*
                          UB_GR_1_2     EQU   0200C[hex]
                          UB_GR_3_4     EQU   0200D[hex]
                          UB_GR_5_6     EQU   0200E[hex]
                          UB_GR_7_8     EQU   0200F[hex]
*
* Start initialization
*
* Set Bit Counter to zero
*
                                        LDAA  #00[hex]
                                        STAA  BIT_CNT
*
* Set User Bits to FF[hex]
*
                                        LDAA  #0FF[hex]
                                        STAA  UB_GR_1_2
                                        STAA  UB_GR_3_4
                                        STAA  UB_GR_5_6
                                        STAA  UB_GR_7_8
*
* Set time 10h 12min 18sec 20fr
*
                                        LDAA  #014[hex]       20 fr
                                        STAA  FRAME
                                        LDAA  #012[hex]       18 sec
                                        STAA  SEC
                                        LDAA  #0C[hex]        12 min
                                        STAA  MIN
                                        LDAA  #0A[hex]        10 hr
                                        STAA  HOUR
*
* Set Format Register
* Format 25 Fr/sec , unused TC bits all set to "0"
*
                                      LDAA  #01[hex]
                                      STAA  TC_FORM_REG
*
* Preset Divide by M+1 Counter
* For the Time Code format 25Fr/sec at nominal speed, the output frequency of the M+1 counter must be 4000Hz.
* If the input frequency is 200kHz, the counter must divide by 50.
* Note that the value M, which must be written into the M Register, is 49.
*
                                      LDAA  #031[hex]       set M to 49
                                      STAA  M_REG_LSB
                                      LDAA  #00[hex]
                                      STAA  M_REG_MSB
*
```

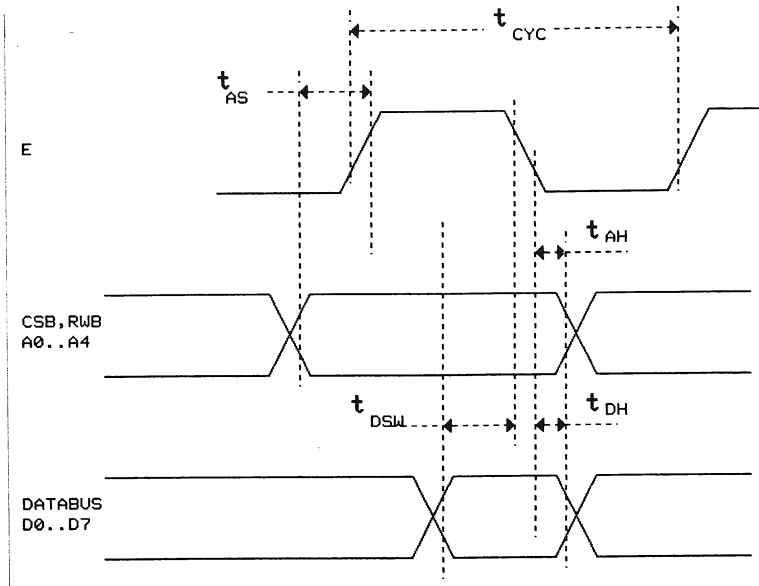
```
*
* Select REFIN1 (M+1 divider output), set forward direction of the Time Code and start the generator
*
                                        LDAA    #01[hex]
                                        STAA    CMD_REG
* END OF ROUTINE
```



Bus Read Timing (Read information from TCGA)

Item	Symbol	min	max	Unit
E Cycle Time	t_{CYC}	200		ns
Address Setup Time	t_{AS}	50		ns
Data Delay Time	t_{DDR}		50	ns
Address Hold Time	t_{AH}	10		ns
Data Hold Time	t_{DH}	10		ns

Fig. 5.: Bus Read Timing Characteristics



Bus Write Timing (Write information into TCGA)

Item	Symbol	min	max	Unit
E Cycle Time	t_{CYC}	200		ns
Address Setup Time	t_{AS}	50		ns
Data Setup Time	t_{DSW}	50		ns
Address Hold Time	t_{AH}	10		ns
Data Hold Time	t_{DH}	10		ns

Fig. 6.: Bus Write Timing Characteristics